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Description

Arrangement for testing a power output stage

The invention relates to an arrangement for testing a power output stage, the power output stage having at least three half-bridges which each comprise a series circuit formed by an upper and a lower semiconductor switch and to which the operating voltage is applied, and the junction points of the semiconductor switches of the half-bridges forming outputs which are connected to windings of an at least three-phase motor.

Power output stages equipped with semiconductor switches are used inter alia in motor vehicles for driving loads, for example motors. By virtue of the rapid development of low-impedance power MOSFETs, even loads in the kilowatts range can be driven cost-effectively. In motor vehicles it can happen that the power output stage and the load are arranged spatially separate from one another, in which case short circuits of the load feed lines to ground or to battery voltage may lead to high fault currents. Fusible links generally cannot be used in these electric circuits on account of their tolerances, their internal resistances and the high useful currents. Moreover, a high fault current may flow on account of a defective MOSFET in the power output stage.

Therefore, it is an object of the invention to provide a testing of the power output stages, so that in the case of a short circuit, the operating voltage is switched off or not even

switched on in the first place, and the power output stage and the on-board electrical system are thus protected against damage.

This object is achieved in the case of the arrangement according to the invention by virtue of the fact that a control device is provided, which switches respectively one or respectively simultaneously a plurality of the semiconductor switches into the on state according to a predetermined program and in the process tests whether the respective voltages at the outputs respectively lie within a predetermined tolerance range for the respective switching state.

The state of the power output stage and of the connected lines and windings can be assessed in differentiated fashion by means of the method according to the invention, the motor not being influenced, or only being imperceptibly influenced, during the testing. The testing may be effected automatically before the power output stage is respectively switched on, for example when the ignition lock of a motor vehicle is actuated, or else may be carried out during operation.

One development of the invention consists in the fact that the feeds to the windings can be interrupted with the aid of further switches. As a result of the isolation of the windings with the aid of the further switches, respectively one to all of the upper semiconductor switches or one to all of the lower semiconductor switches can be simultaneously controlled into the on state, so that a precise fault analysis is possible.

One advantageous refinement of the invention consists in the fact that the windings of the motor form a star connection, and that the further switches are arranged at the star point and in the

feed lines, from the outputs to the windings. Although other controllable switches are also suitable for the arrangement according to the invention, it is preferably provided in the case of the arrangement according to the invention that the further switches are relays. The invention can also be applied to delta-connected windings.

Since the operating voltage of the power output stages is generally significantly higher than that of microprocessors or digital signal processors, in one advantageous refinement of the arrangement according to the invention provision is made of connections of the outputs of the half-bridges and of the operating voltage to inputs of window comparators via voltage dividers.

In order to ensure a reproducible voltage at the outputs when semiconductor switches are switched off, in the case of the method according to the invention means may be provided which have the effect that when semiconductor switches are not in the on state, the respective output voltage lies within the predetermined average tolerance range.

This development is preferably configured in such a way that the means are formed by a resistor, which is located between the output of one of the half-bridges and the operating voltage source and generates together with the voltage divider at the output a voltage in the average tolerance range.

In one development of the arrangement according to the invention, testing without an overloading of the power output stage and of the devices for voltage supply is possible by virtue of the fact that a controllable switch is provided

in the feed line of the operating voltage, a resistor being connected in parallel with said controllable switch, and in that the controllable switch can be controlled by the control device. As an alternative, in the case of the arrangement according to the invention it may be provided that the pulses serving for testing are so short that no overloading of the semiconductor switches takes place and, moreover, the load is not influenced or is only imperceptibly influenced during the testing.

The invention permits numerous embodiments. One of them is illustrated schematically in the drawing and described below.

In the case of the exemplary embodiment illustrated, two MOSFETs 1, 2; 3, 4; 5, 6 respectively form a half-bridge 7, 8, 9 having outputs 10, 11, 12, to which one of the star-connected windings 13, 14, 15 of a motor is respectively connected. Contacts of a relay 31 are located in the feed lines to the windings 13, 14, 15. In addition, the start point can be interrupted with the aid of a further relay 32.

The operating voltage Ubat is fed to an input 16, and is fed as U+ via a relay 17 to the power output stage. Connected in parallel with the relay 17 is a current limiting resistor 18, via which an electrolytic capacitor 19 having a high capacitance can be charged, the relay only being switched on if the voltage U+ approximately corresponds to the voltage Ubat. An impermissibly high charging current surge is thus avoided. Details concerning this known circuit are explained in DE 100 57 156 A1.

The arrangement furthermore comprises a control device 20, which is known as such in connection with power output stages, is formed by a microcomputer or a digital signal processor and as such need not be explained in any greater detail for an understanding of the invention. Outputs of the control device 20 are connected to a drive circuit 21, which generates control signals HS1, HS2, HS3, LS1, LS2, LS3 for the MOSFETs 1 to 6. Analog/digital converters 20' are furthermore connected to the control device 20, and voltages generated by a respective voltage divider 22, 23, 24, 25 can be fed to the inputs of said converters. The voltage dividers have significantly higher resistance values than the windings 13, 14, 15 in order not to impair the efficiency of the output stage during operation. In addition, coils of the relays 31, 32 are connected to outputs of the control device 20.

A resistor 26 is connected in parallel with the MOSFET 1, which resistor, together with the voltage divider 23, has the effect that half of the voltage U+ is present at the output 10 of the half-bridge 7 in the case of MOSFETs 1, 2 that are not in the on state.

The voltage dividers 22 to 25 are designed in such a way that at the highest possible value of U+, the permissible voltage of CMOS circuits is not exceeded. The voltage generated by the voltage divider 22 serves for the individual tests described below as a voltage reference for forming the tolerance ranges.

During the first test, with contacts of the relay 31 which are initially open, the MOSFETs 1 to 6 are not driven, so that the output 10 carries the voltage U+/2, which is checked in the control device 20 whilst taking account

of a predetermined tolerance. If this is the case, it can be deduced from this that no short circuit to ground 27 or operating voltage U+ is present in the MOSFETs 1, 2 and in the feed line up to the relay 31. In the case where the power output stage is free of faults, the MOSFETs 3 to 6 are also not in the on state during this first test, so that when the contacts of the relay 31 are subsequently closed via the windings 13 to 15 of the motor, the voltages at the outputs 11, 12 likewise lie within the average tolerance range, which is tested by the control device 20.

During another test, the "upper" MOSFETs 1, 3, 5 are successively switched into the on state and in the process a check is respectively made to determine whether the outputs 10, 11, 12 assume a voltage lying within an upper tolerance range, that is to say in the vicinity of the voltage U+. During a further test, the "lower" MOSFETs 2, 4, 6 are successively brought to the on state. In this case, a check is respectively made to determine whether the voltage at the outputs 10, 11, 12 lies within the lower tolerance range, that is to say - compared with U+ - in the vicinity of the ground potential. These tests may be performed successively with closed and opened contacts of the relays 31, 32.

By virtue of the arrangement of the relays, it is possible, for test purposes, to switch respectively one, two or all of the upper and lower semiconductor switches into the on state and to observe the behavior of the voltages at the outputs. The type and the location of the defect, for example short circuit, overloading or relay defects, can be deduced from the magnitude by which the respective tolerance range is exceeded or undershot.